This listing of claims will replace all prior version, and listing, of claims in the application :

Claim 1 (currently amended) : An integrated circuit package having central leads comprising:

a substrate having an upper surface, a lower surface and a long slot penetrating from the upper surface to the lower surface, the lower surface forming with wiring regions arranged at the two sides of the long slot, and the wiring regions forming with a plurality of connected points, the length of the wiring regions are smaller than long slot of the substrate ;

a resistant layer42 is coated on the lower surface54 of the substrate40, and is located between the long slot56 and wiring region58

a glue layer being coated on the upper surface of the substrate and being located at the periphery of the long slot ;

an integrated circuit having a first surface forming with a plurality of bonding pads and a second surface, the first surface being adhered to the glue layer, then the bonding pads being exposed from the long slot of the substrate ;

a plurality of wires, each of which is arranged within the long slot of the substrate and is electrically connected the bonding pad of the integrated circuit to the connected point of the substrate ; and

a first compound layer being filled within the long slot of the substrate for

protecting the each wire.

Claim 2 (original) : The integrate circuit package having central leads according to claim 1, wherein the length of the wiring regions are shorter than the long slot of the substrate

Claim 3 (currently amended) : The integrate circuit package having central leads according to claim 1, wherein the connected points of the lower surface of the substrate is are formed with ball grid array (BGA).

Claim 4 (original) : The integrate circuit package having central leads according to claim 1, wherein further comprises a second compound layer, which is covered on the upper surface of the substrate.